Electronic Version
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[NAND FLASH MEMORY CELL ROW, NAND FLASH MEMORY CELL ARRAY, OPERATION AND FABRICATION METHOD THEREOF]

Abstract

A NAND flash memory cell array including a plurality of memory cell row is provided. Each of memory cell row includes a plurality of memory cells disposed between first selecting transistor and second selecting transistor connected in series. Each memory cell has a tunneling dielectric layer, a floating gate, an inter-gate dielectric, a control gate and source/drain regions. An erase gate is disposed between two adjacent memory cells. A plurality of word lines serve to connect the memory cells in rows. A source line serves to connect the source region of the first transistor in a row, whereas a plurality of bit lines serve to connect the drain region of second transistor in a row. A first selecting gate line and a second selecting gate line serve to connect the gate of the first transistor in a row and the gate of second transistor in a row respectively. A plurality of erase gate lines is connected to the erase gates in a

row.